AMENDMENT TO THE CLAIMS

Applicants selectively amend the claims as follows:

Listing of Claims:

- 1 1. (Currently Amended) An apparatus, comprising:
- a data path input unit to receive a packet from a transmitting device that does not
- 3 <u>expect a completion acknowledgement</u> for a request transaction that does not expect a
- 4 completion; and
- a data path output unit to transmit a message to the transmitting device if the
- 6 request transaction is unsuccessful.
- 1 2. (Original) The apparatus of claim 1, the packet including a packet header that includes
- 2 a requester identification field that identifies the transmitting device.
- 1 3. (Original) The apparatus of claim 2, the contents of the requester identification field
- 2 used to route the message back to the transmitting device.
- 4. (Currently Amended) The apparatus of claim 3, the message including an unsuccessful
- 2 <u>unsupported</u> request error message.

5. (Original) The apparatus of claim 3, the message including an undefined packet error 1 2 message. 6. (Original) The apparatus of claim 3, the message including a malformed packet error 1 2 message. 1 7. (Currently Amended) A system, comprising: 2 a transmitting device to transmit a packet for a request transaction-that, wherein the transmitting device does not expect a completion acknowledgement; and 3 4 a receiving device to receive the packet and to return a message to the transmitting device if the request transaction is unsuccessful. 5 8. (Original) The system of claim 7, the packet including a packet header that includes a 1 requester identification field that identifies the transmitting device. 2 9. (Original) The system of claim 8, the contents of the requester identification field used 1 2 to route the message back to the transmitting device. 10. (Currently Amended) The system of claim 9, the message including an unsuccessful 1 unsupported request error message. 2 11. (Original) The system of claim 9, the message including an undefined packet error 1

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message.

12. (Original) The system of claim 9, the message including a malformed packet error 1 2 message. 1 13. (Currently Amended) A method, comprising: 2 receiving a request packet from a transmitting device; 3 determining whether an error condition exists; and if an error condition exists and the request packet does not indicate[[s]] that a 4 completion acknowledgement is not expected, delivering an error message to the 5 6 transmitting device. 1 14. (Currently Amended) The method of claim 13, further comprising delivering a completion packet with a non-successful completion status to the transmitting device if 2 an error condition exists and the request packet indicates that a completion 3 acknowledgement is expected. 4 15. (Original) The method of claim 14, wherein the error message indicates an undefined 1 2 packet. 16. (Original) The method of claim 14, wherein the error message indicates a malformed 1 2 packet. 17. (Original) The method of claim 14, wherein the error message indicates an 1

unsupported request.

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- 1 18. (New) A system, comprising:
- a requesting device to transmit a packet for a memory transaction over one or
- 3 more point-to-point communication links, wherein the requesting device does not expect
- 4 a completion acknowledgement; and
- a completing device to receive the packet and to return a message to the
- 6 requesting device if the memory transaction is unsuccessful.
- 1 19. (New) The system of claim 18, the packet including a packet header that includes a
- 2 requester identification field that identifies the requesting device.
- 1 20. (New) The system of claim 19, the contents of the requester identification field used
- 2 to route the message back to the requesting device.
- 1 21. (New) The system of claim 19, the message including an unsupported request error
- 2 message.
- 1 22. (New) The system of claim 19, the message including an undefined packet error
- 2 message.
- 1 23. (New) The system of claim 19, the message including a malformed packet error
- 2 message.

- 1 24. (New) The system of claim 18, the memory transaction including a memory write
- 2 transaction.